

NCV8163

Product Preview

250 mA, Ultra-Low Noise and High PSRR LDO Regulator for RF and Analog Circuits

The NCV8163 is a next generation of high PSRR, ultra-low noise LDO capable of supplying 250 mA output current. Designed to meet the requirements of RF and sensitive analog circuits, the NCV8163 device provides ultra-low noise, high PSRR and low quiescent current. The device also offer excelent load/line transients. The NCV8163 is designed to work with a 1 μ F input and a 1 μ F output ceramic capacitor. It is available in XDFN4 0.65P, 1 mm x 1 mm package.

Features

- Operating Input Voltage Range: 2.2 V to 5.5 V
- Available in Fixed Voltage Option: 1.2 V to 5.3 V
- $\pm 2\%$ Accuracy Over Load/Temperature
- Ultra Low Quiescent Current Typ. 12 μ A
- Standby Current: Typ. 0.1 μ A
- Very Low Dropout: 80 mV at 250 mA
- Ultra High PSRR: Typ. 92 dB at 20 mA, $f = 1$ kHz
- Ultra Low Noise: 6.5 μ V_{RMS}
- Stable with a 1 μ F Small Case Size Ceramic Capacitors
- Available in XDFN4 1 mm x 1 mm x 0.4 mm package
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; Grade 1 AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Parking Cameras Modules
- Wireless Handsets, Wireless LAN, Bluetooth, Zigbee
- Automotive Infotainment Systems
- Other Battery-Powered Applications

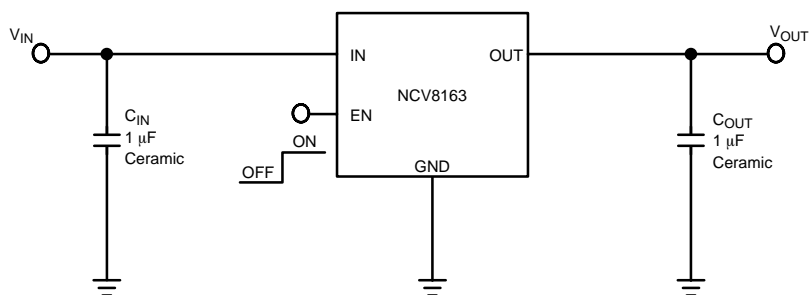


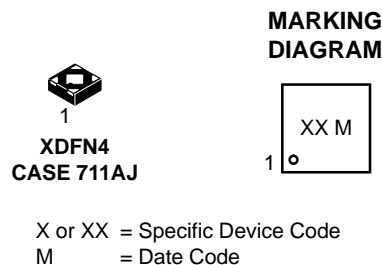
Figure 1. Typical Application Schematics

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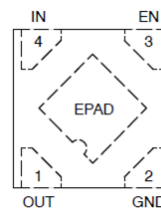


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PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 6 of this data sheet.

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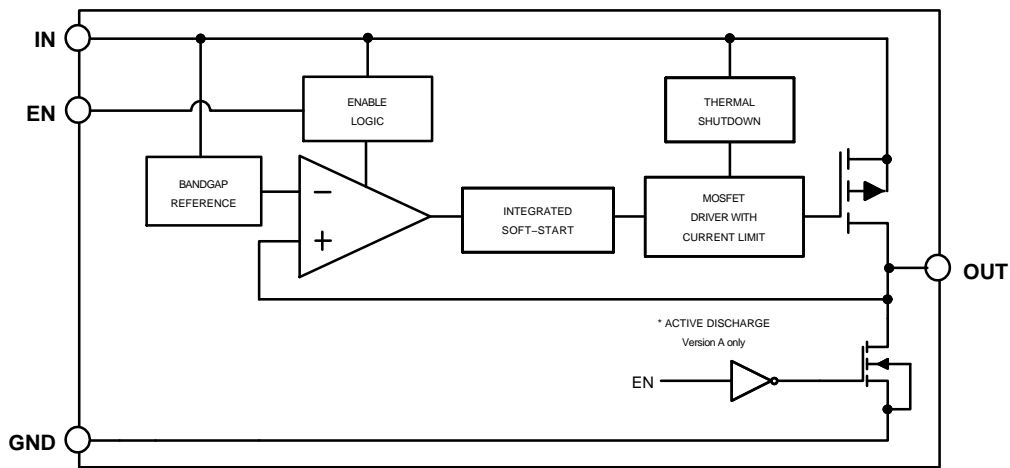


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
4	IN	Input voltage supply pin
1	OUT	Regulated output voltage. The output should be bypassed with small 1 μ F ceramic capacitor.
3	EN	Chip enable: Applying $V_{EN} < 0.4$ V disables the regulator, Pulling $V_{EN} > 1.2$ V enables the LDO.
2	GND	Common ground connection
EPAD	EPAD	Expose pad can be tied to ground plane for better power dissipation

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	-0.3 V to 6	V
Output Voltage	V_{OUT}	-0.3 to $V_{IN} + 0.3$, max. 6 V	V
Chip Enable Input	V_{CE}	-0.3 to $V_{IN} + 0.3$, max. 6 V	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Operating Ambient Temperature Range	T_A	-40 to +125	$^{\circ}$ C
Maximum Junction Temperature	T_J	150	$^{\circ}$ C
Storage Temperature Range	T_{STG}	-55 to +150	$^{\circ}$ C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
 - ESD Human Body Model tested per EIA/JESD22-A114
 - ESD Machine Model tested per EIA/JESD22-A115
 - ESD Charged Device Model tested per EIA/JESD22-C101, Field Induced Charge Model
 - Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Input Voltage	V_{IN}	2.2	5.5	V
Junction Temperature	T_J	-40	+125	$^{\circ}$ C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, XDFN4 (Note 3), Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	198.1	$^{\circ}$ C/W

3. Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51-7

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ELECTRICAL CHARACTERISTICS $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$; $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$; $I_{OUT} = 1\text{ mA}$, $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$, unless otherwise noted. $V_{EN} = 1.2\text{ V}$. Typical values are at $T_J = +25^{\circ}\text{C}$ (Note 4).

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage		V_{IN}	2.2		5.5	V
Output Voltage Accuracy	$V_{IN} = (V_{OUT(NOM)} + 1\text{ V})$ to 5.5 V	V_{OUT}	-2		+2	%
	$V_{IN} = (V_{OUT(NOM)} + 1\text{ V})$ to 5.5 V (for $V_{OUT} < 1.8\text{ V}$)	V_{OUT}	-3		+3	%
Line Regulation	$V_{OUT(NOM)} + 1\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	$Line_{Reg}$		0.02		%/V
Load Regulation	$I_{OUT} = 1\text{ mA}$ to 250 mA	$Load_{Reg}$		0.001	0.005	%/mA
Dropout Voltage (Note 5)	$I_{OUT} = 250\text{ mA}$	V_{DO}		180	250	mV
				110	175	
				95	160	
				90	155	
				80	145	
				75	105	
Output Current Limit	$V_{OUT} = 90\% V_{OUT(NOM)}$	I_{CL}	250	700		mA
Short Circuit Current	$V_{OUT} = 0\text{ V}$	I_{SC}		690		
Quiescent Current	$I_{OUT} = 0\text{ mA}$	I_Q		12	20	μA
Shutdown Current	$V_{EN} \leq 0.4\text{ V}$, $V_{IN} = 4.8\text{ V}$	I_{DIS}		0.01	1	μA
EN Pin Threshold Voltage	EN Input Voltage "H"	V_{ENH}	1.2			V
	EN Input Voltage "L"	V_{ENL}			0.4	
EN Pull Down Current	$V_{EN} = 4.8\text{ V}$	I_{EN}		0.2	0.5	μA
Turn-On Time	$C_{OUT} = 1\text{ }\mu\text{F}$, From assertion of V_{EN} to $V_{OUT} = 95\% V_{OUT(NOM)}$			120		μs
Power Supply Rejection Ratio	$I_{OUT} = 20\text{ mA}$	PSRR	$f = 100\text{ Hz}$	91	dB	
			$f = 1\text{ kHz}$	92		
			$f = 10\text{ kHz}$	85		
			$f = 100\text{ kHz}$	60		
Output Voltage Noise	$f = 10\text{ Hz}$ to 100 kHz	V_N		8.0 6.5		μV_{RMS}
Thermal Shutdown Threshold	Temperature rising	T_{SDH}		160		$^{\circ}\text{C}$
	Temperature falling	T_{SDL}		140		$^{\circ}\text{C}$
Active Output Discharge Resistance	$V_{EN} < 0.4\text{ V}$, Version A only	R_{DIS}		280		Ω
Line Transient (Note 6)	$V_{IN} = (V_{OUT(NOM)} + 1\text{ V})$ to $(V_{OUT(NOM)} + 1.6\text{ V})$ in 30 μs , $I_{OUT} = 1\text{ mA}$	$Tran_{LINE}$	-1			mV
	$V_{IN} = (V_{OUT(NOM)} + 1.6\text{ V})$ to $(V_{OUT(NOM)} + 1\text{ V})$ in 30 μs , $I_{OUT} = 1\text{ mA}$				+1	
Load Transient (Note 6)	$I_{OUT} = 1\text{ mA}$ to 200 mA in 10 μs	$Tran_{LOAD}$	-40			mV
	$I_{OUT} = 200\text{ mA}$ to 1mA in 10 μs				+40	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_A = 25^{\circ}\text{C}$.

Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.

5. Dropout voltage is characterized when V_{OUT} falls 100 mV below $V_{OUT(NOM)}$.

6. Guaranteed by design.

APPLICATIONS INFORMATION

General

The NCV8163 is an ultra–low noise 250 mA low dropout regulator designed to meet the requirements of RF applications and high performance analog circuits. The NCV8163 device provides very high PSRR and excellent dynamic response. In connection with low quiescent current this device is well suitable for battery powered application such as cell phones, tablets and other. The NCV8163 is fully protected in case of current overload, output short circuit and overheating.

Input Capacitor Selection (C_{IN})

Input capacitor connected as close as possible is necessary for ensure device stability. The X7R or X5R capacitor should be used for reliable performance over temperature range. The value of the input capacitor should be 1 μF or greater to ensure the best dynamic performance. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes.

Output Decoupling (C_{OUT})

The NCV8163 requires an output capacitor connected as close as possible to the output pin of the regulator. The recommended capacitor value is 1 μF and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. The NCV8163 is designed to remain stable with minimum effective capacitance of 0.7 μF to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0201 the effective capacitance drops rapidly with the applied DC bias. Please refer Figure 3.

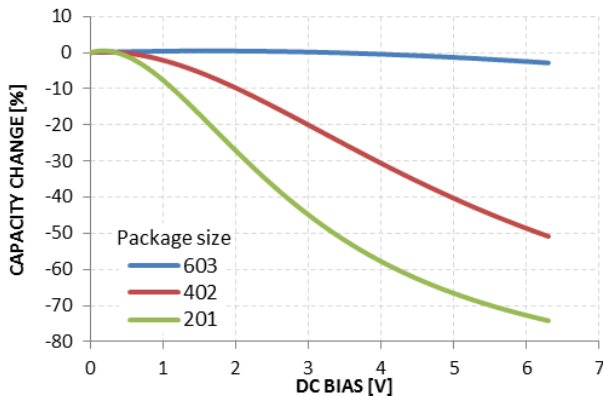


Figure 3. Capacity vs DC Bias Voltage

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 2 Ω. Larger output capacitors and lower ESR could improve the load

transient response or high frequency PSRR. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature.

Enable Operation

The NCV8163 uses the EN pin to enable/disable its device and to deactivate/activate the active discharge function.

If the EN pin voltage is <0.4 V the device is guaranteed to be disabled. The pass transistor is turned–off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active so that the output voltage V_{OUT} is pulled to GND through a 280 Ω resistor. In the disable state the device consumes as low as typ. 10 nA from the V_{IN}.

If the EN pin voltage >1.2 V the device is guaranteed to be enabled. The NCV8163 regulates the output voltage and the active discharge transistor is turned–off.

The EN pin has internal pull–down current source with typ. value of 200 nA which assures that the device is turned–off when the EN pin is not connected. In the case where the EN function isn’t required the EN should be tied directly to IN.

Output Current Limit

Output Current is internally limited within the IC to a typical 700 mA. The NCV8163 will source this amount of current measured with a voltage drops on the 90% of the nominal V_{OUT}. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current to 690 mA (typ). The current limit and short circuit protection will work properly over whole temperature range and also input voltage range. There is no limitation for the short circuit duration.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (T_{SD} – 160°C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (T_{SDU} – 140°C typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipated in the NCV8163 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the

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ambient temperature affect the rate of junction temperature rise for the part.

The maximum power dissipation the NCV8163 can handle is given by:

$$P_{D(MAX)} = \frac{[125^{\circ}\text{C} - T_A]}{\theta_{JA}} \quad (\text{eq. 1})$$

The power dissipated by the NCV8163 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN} \cdot I_{GND} + I_{OUT}(V_{IN} - V_{OUT}) \quad (\text{eq. 2})$$

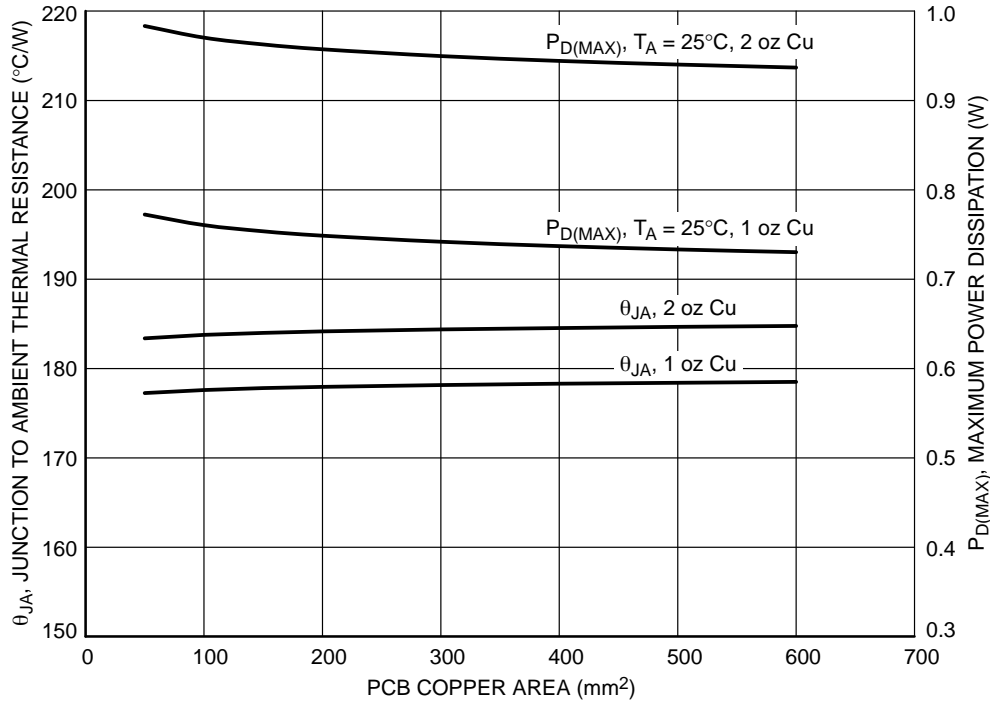


Figure 4. θ_{JA} and $P_D (MAX)$ vs. Copper Area

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Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Power Supply Rejection Ratio

The NCV8163 features very high Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

Turn-On Time

The turn-on time is defined as the time period from EN assertion to the point in which V_{OUT} will reach 98% of its nominal value. This time is dependent on various application conditions such as $V_{OUT(NOM)}$, C_{OUT} , T_A .

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 or 0201 capacitors with appropriate capacity. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 2). Expose pad can be tied to the GND pin for improvement power dissipation and lower device temperature.

ORDERING INFORMATION

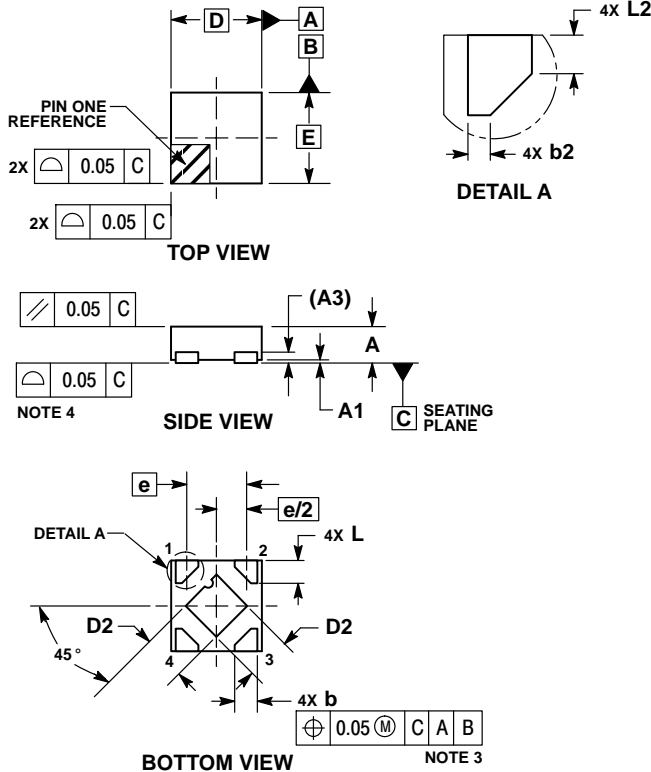
Device	Voltage Option	Marking	Description	Package	Shipping†
NCV8163AMX120TBG	1.2 V	ME	250 mA, Active Discharge	XDFN4 CASE 711AJ (Pb-Free)	3000 / Tape & Reel
NCV8163AMX150TBG	1.5 V	MV			
NCV8163AMX180TBG	1.8 V	MA			
NCV8163AMX250TBG	2.5 V	MU			
NCV8163AMX270TBG	2.7 V	MX			
NCV8163AMX280TBG	2.8 V	MM			
NCV8163AMX300TBG	3.0 V	MJ			
NCV8163AMX330TBG	3.3 V	MK			

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

XDFN4 1.0x1.0, 0.65P CASE 711AJ ISSUE A

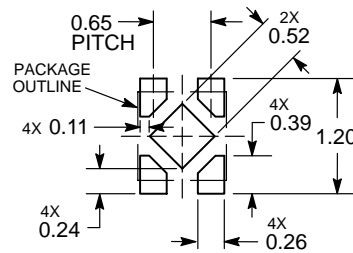


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM THE TERMINAL TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.33	0.43
A1	0.00	0.05
A3	0.10 REF	
b	0.15	0.25
b2	0.02	0.12
D	1.00 BSC	
D2	0.43	0.53
E	1.00 BSC	
e	0.65 BSC	
L	0.20	0.30
L2	0.07	0.17

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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